A Novel HVDC Circuit Breaker for HVDC Application

Meng Zhou, Wang Xiang, Wenping Zuo, Weixing Lin, Jinyu Wen

***Abstract*—Hybrid high voltage direct current circuit breakers (DCCBs) are capable of interrupting fault current within a few milliseconds, but this technology has high capital cost, especially in a meshed HVDC grid. To increase the economic competitiveness of hybrid DCCBs, this paper proposes a capacitor commutated dc circuit breaker (CCCB). The CCCB mainly comprises an auxiliary branch with a fast dis-connector in series with semiconductor devices and the main branch with the series connection of a dc capacitor and diode valves. This paper provides a detailed depiction of the CCCB. The topology and operating principles are discussed. The impact of snubber circuits and stray inductances on the commutation process is analyzed. The general sizing method for the main components in the CCCB is detailed. Reclosing to transmission lines with different operating conditions is studied. Several extended topologies are proposed to further reduce the semiconductor cost and on-state operation power loss. The power loss and cost of CCCB are assessed. Extensive simulations on PSCAD/EMTDC verified the dc fault isolation and reclosing of the CCCB.**

***Index Terms*—DC circuit breaker, dc grids, HVDC converters, HVDC transmission**

I. Introduction

In recent years, there has been great interest in developing a multi-terminal HVDC system (MTDC) and dc grids. The dc circuit breaker (DCCB) is one of the most important components in a dc grid[1][2]. Various DCCB topologies have been reported in [3]-[21]. Depending on the interrupting method, DCCB technologies can be classified into three categories: the solid-state DCCBs, the hybrid DCCBs, and the mechanical DCCBs.

The solid-state DCCB has high cost and high power loss and is not competitive for HVDC application [1]. The active resonant mechanical DCCBs reported in [3]-[7] utilize inductors and pre-charged capacitors to create a zero current to interrupt the fault current. The power loss of mechanical DCCBs is almost negligible since only the vacuum circuit breaker (VCB) is exposed to line dc current during normal operation. Typically, an interrupter, such as a VCB, driven by a hydraulic actuator with an operation time of approximately *15ms* is used at the main branch in a traditional active resonant mechanical DCCB [3]. Consequently, the break operation time [8] (time interval between the reception of the trip order and the beginning of the rise of the transient interrupting voltage) of this traditional mechanical DCCB is too long to meet the requirement of fast fault current interruption. Reference [4] reported a mechanical DCCB that can interrupt dc current of up to *16kA* within *10ms*. To accelerate the operation speed of the interrupter, an electromagnetic actuator is introduced. References [5]-[6] demonstrated active resonant mechanical DCCBs driven by electromagnetic actuator that can interrupt dc fault current of up to *16kA* within 5ms. However, it might be technologically challenging to achieve fast auto-reclose within 200-500ms[7] for mechanical DCCBs since the capacitors need to be recharged.

To combine the advantages of solid-state DCCBs and mechanical DCCBs, hybrid DCCBs were proposed in [9]-[21]. References [9]-[10] developed a prototype that achieved a current breaking capability as high as 9kA in a dc test system with rated dc voltage of 320kV and rated dc current of 2kA. The load commutation switch (LCS) in a hybrid HVDC breaker was assessed in [11]. To facilitate dc grid level studies, the modeling principles and coordinated control of the hybrid DCCB were analyzed in [12]. A similar technology proposed in [13] utilizes a large number of cascaded full bridge sub-modules instead of IGBTs connected in series to form the main branch. This technology was able to interrupt dc fault current up to 15kA within 3ms under a voltage rating of 200kV. A hybrid DCCB with its main branch composed of thyristors in series with capacitors was presented in [14]. The number of sub-units of this technology is large, which increases the complexity of the control system. A novel hybrid DCCB based on the arc voltage instead of the use of power electronics in the auxiliary branch was presented in [15]. Experimental prototype test results showed that it can interrupt fault current of up to 10kA within 5ms.

Another design scheme for hybrid DCCB was proposed in [19]. It replaces the main branch with an un-charged capacitor and is economically competitive. However, the detailed design, operation principles and verifications were not presented. A capacitor-buffering DCCB was depicted in [20]. When operating in arc mode, the number of power electronic devices can be significantly decreased. However, the reliability needs to be studied in detail. A thyristor-based hybrid arc-less DCCB was proposed in [21]. Compared with the hybrid DCCB proposed in [9], it can reduce the number of IGBT devices, but a large number of IGBTs remains unavoidable.

To reduce the cost of DCCB, several publications used the idea of sharing the main breaker branch between several circuit breakers, such as the interlink DCCB and multiport DCCBs [16]-[18]. However, these DCCBs are dedicated to a connection point with multiple DC lines. And the main branch

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topology can still be improved.

In summary, the main branch of the hybrid DCCB topologies proposed in [9]-[13] contains large number of power electronic devices, which results in high cost.

To solve the problems mentioned above, this paper proposes a capacitor commutated DC circuit breaker (CCCB). A commutated capacitor is adopted in the main branch to reduce the cost. The topology and operating principle of CCCB are analyzed. Several extended CCCB topologies are designed to meet different application scenarios. The parameters of the internal components of the CCCB are dimensioned. The power loss and cost are evaluated. Finally, the performance and effectiveness of the CCCB are verified by extensive simulations in PSCAD/EMTDC.

II. Topology of the Capacitor Commutated DCCB

A. Topology and Operating Principle of the CCCB

Fig. 1 shows the basic topology of the CCCB. It includes an auxiliary branch composed of a load commutation switch (LCS) in series with an ultra-fast disconnector (UFD) S_1, a main branch formed by a commutated capacitor C in series with a diode valve D, an arrester bank, a residual switch S_2 and a discharging branch composed of residual switch S_3 in series with resistor R. To provide sufficient commutation voltage at low power loss, the LCS is consisted of 3x3 matrix of IGBTs with parallel RCD snubbers. The snubber circuits are used to reduce the voltage spikes across the T_1 during the switching period [11].

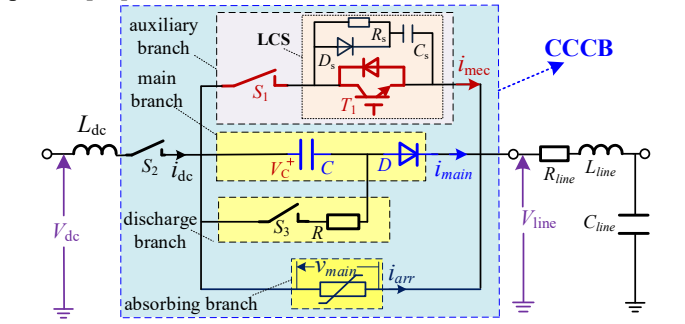


Fig. 1 Basic topology of a unidirectional capacitor commutated DCCB (CCCB)

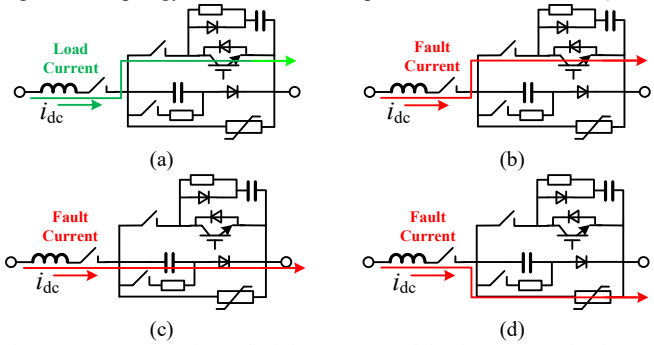


Fig. 2 CCCB operation principle. (a) Normal load current path. (b) Fault initiates operation. (c) LCS interrupts and commutates current to main branch. (d) Main branch interrupts and commutates current to the arrester.

Fig. 2 shows the operation principle of CCCB. During normal operation, S_2, UFD, T_1 are closed and S_3 is opened. The load current i_{dc} only flows through the auxiliary branch. The green line in Fig. 2(a) shows the load current path during this phase. When DC faults occur, i_{dc} increases and flows through the auxiliary branch, as shown in Fig. 2(b). Upon receiving a trip order, the LCS is firstly turned off. Then i_{dc} is sequentially commutating from the auxiliary branch to the main branch. When i_{dc} is successfully commutated into the main branch, the i_{mec} in auxiliary branch decreases to zero. Meanwhile, the order to open UFD (S_1) is sent. Therefore, the UFD can be tripped at zero current after the delay of commutation time $\Delta t_{\mathrm{AB\text{-}MB}}$ (the time i_{dc} commutates from the auxiliary branch (AB) to the main branch (MB)). At this time, the i_{dc} will charge the commutated capacitor located in the main branch. Fig. 2(c) illustrates the commutated current path in the main branch. When the commutated capacitor is charged to exceed the threshold voltage of arrester banks, i_{dc} will transfer to the absorbing branch. Finally, the fault energy stored in the DC system will be dissipated by the arrester banks, as shown in Fig. 2(d).

A duration time of ΔT (typically 2ms[11]) is required for the contacts of UFD to reach sufficient dielectric distance. During ΔT, i_{dc} charges C. The capacitor voltage V_c is undertaken by UFD and T_1 together. After the successful opening of the UFD, V_c is withstood by UFD. Once V_c is higher than V_{dc}, the dc current starts to decrease.

When V_c increases to the protective level of the arrester, the dc current in the main branch i_{main} is totally commutated to the absorbing branch. Because the capacitor C cannot discharge through diode D, the peak value of V_c is maintained at the protective level of the arrester. When i_{dc} is less than the chopper threshold of S_2, S_2 will be opened to interrupt the residual current flowing through the arrester.

To enable the fast reclosing of a CCCB in case of transient dc fault, S_2 may not need to be opened after isolating the dc fault. After detecting that V_{line} is higher than a certain threshold for a minimum duration, the dc fault is deemed isolated, and S_3 will be closed to discharge the dc capacitor. Once the current through S_3 is lower than the chopping margin of S_3, S_3 will be opened. Then, the order to reclose the CCCB will be sent.

B. Dynamics during Opening of the CCCB

In normal operation, the dc current i_{dc} only flows through the auxiliary branch. The voltage across the commutated capacitor, V_{c0}, equals to the voltage drop across T_1, which is expressed as

$$V_{c0} = V_{CE0\_T1} + R_{T1} i_{dc} \tag{1}$$

where V_{CE0_T1} and R_{T1} are the equivalent threshold voltage and equivalent on-state resistance of T_1, respectively. Typically, V_{c0} is on the order of several tens of volts since V_{CE0_T1} and R_{T1} are considerably small.

Once receiving the trip order, T_1 is turned off. The fault current will charge the snubber circuits. Once the snubber capacitor voltage reaches its peak value, i_{mec} will commutate to the main branch. During the short commutation period $\Delta t_{AB\text{-}MB}$, as the current rise rate is limited by the current limiting inductance, the i_{dc} is assumed to be constant. Therefore, we have

$$i_{main} + i_{mec} = I_{dctrip} \tag{2}$$

$$\frac{di_{main}}{dt} + \frac{di_{mec}}{dt} = \frac{di_{dc}}{dt} = 0 \tag{3}$$

where I_{dctrip} is the dc current at the moment when the trip order of CCCB is sent.

When the commutation process from auxiliary branch to main branch is completed, the commutated capacitor C will be charged. Simultaneously, the UFD starts to open its contact because the i_{mec} has decreased to zero. Neglecting the fault resistance R_{flt} and the resistance and inductance (R_{line}, L_{line}) of transmission line, the equations during the charging of C is

$$\begin{cases} V_{dc} = L_{dc}\dfrac{di_{dc}}{dt} + L_{sMB}\dfrac{di_{main}}{dt} + V_c, i_{dc} > 0 \\ V_c = V_{c0} + \dfrac{1}{C}\int i_{main}dt \approx \dfrac{1}{C}\int i_{dc}dt \end{cases} \quad (4)$$

where L_{dc} is the current limiting reactor. L_{sMB} is the stray inductance of the main branch. The V_{c0} is relatively small and can therefore be ignored. Assuming that the CCCB receives a trip order at t=0, from (4), the analytical expressions of i_{dc} and V_c during the internal current commutation time [8] (the time interval between the reception of the trip order and the instant when the fault current starts to decrease) are as follows:

$$i_{dc} = I_{dctrip}\cos(\omega_0 t) + V_{dcn}\sin(\omega_0 t)/Z_c \quad (5)$$

$$V_c = Z_c I_{dctrip}\sin(\omega_0 t) + V_{dcn}[1-\cos(\omega_0 t)] \quad (6)$$

where $Z_c = \sqrt{(L_{dc}+L_{sMB})/C}, \omega_0 = 1/\sqrt{(L_{dc}+L_{sMB})C}$.

C. Impact of the Commutation Capacitance on the Peak Fault Current

Assume the dc voltage at the dc bus is maintained at rated value. The dc fault current i_{dc} reaches its peak value when V_c equals to V_{dcn}. The instant T_{peak} when $V_c = V_{dcn}$ is obtained from solving the equation (6). The peak of i_{dc} is calculated from

$$I_{dcpeak} = I_{dctrip}\cos(\omega_0 T_{peak}) + V_{dcn}\sin(\omega_0 T_{peak})/Z_c \quad (7)$$

Fig. 3 shows the peak fault current I_{dcpeak} versus different commutation capacitances. Parameters for the tested CCCB are listed in Table 4, except that C is varied from 40μF to 100μF. The larger the commutation capacitance C, the higher the peak fault current I_{dcpeak}. The peak fault current is approximately to 8kA if the commutated capacitance is designed as 60μF.

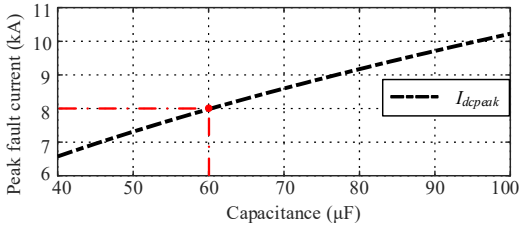


Fig. 3 Peak fault current versus different commutated capacitances

D. Impact of Snubbers on Commutation Time between the Auxiliary Branch and the Main Branch

Fig. 4 shows the equivalent circuit of CCCB at the moment when the T_1 has been turned off.

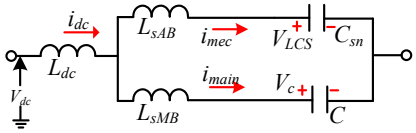


Fig. 4 CCCB equivalent circuit for commutation time of $\Delta t_{AB\text{-}MB}$. (after T_1 is turned off)

The equivalent circuit demonstrated in Fig. 4 is only valid from the moment when the T_1 is turned off to the moment when the i_{mec} decreases to zero. The equivalent RCD snubbers for LCS are simplified as C_{sn} after T_1 is turned off. L_{sAB} is the stray inductance of the auxiliary branch. L_{sMB} is the stray inductance of the main branch. The i_{mec}, after T_1 is turned off, can be calculated using the following equation:

$$i_{mec} = I_{dctrip}\cos(\omega_{mec}t) + \frac{1}{\omega_{mec}}\frac{di_{dc}}{dt}\sin(\omega_{mec}t) \quad (8)$$

where $\omega_{mec} = 1/\sqrt{L_{sAB}C_{snequ}}$. The equivalent snubber capacitance C_{snequ} of LCS is calculated as

$$C_{snequ} = C_{sn}/N_{sn} \quad (9)$$

where the N_{sn} is the number of snubbers connected in series. The snubber capacitance used for each IGBT is defined as C_{sn}. The RCD snubber used for each IGBT in the LCS is set to 8Ω/5μF[23][24]. The i_{dc} is successfully commutated to main branch when i_{mec} decreases to zero. The commutation time of $\Delta t_{AB\text{-}MB}$ is obtained by solving the following equation.

$$\Delta t_{AB\text{-}MB} = \frac{0.5}{\omega_{mec}}\left[\pi - \arctan\left(\frac{di_{dc}}{dt}\frac{1}{\omega_{mec}I_{dctrip}}\right)\right] \quad (10)$$

From equation (10), it can be seen that the snubber capacitor C_{sn} and stray inductance L_{sAB} determine the commutation time of $\Delta t_{AB\text{-}MB}$. Depending on the different DCCB concepts, the typical value of $\Delta t_{AB\text{-}MB}$ varies from 16μs [22] to 250μs [11]. As the capacitance of C in main branch is much larger than the equivalent snubber capacitance C_{snequ}, a fast commutation can be achieved by optimized design of the snubbers of LCS. The snubbers have to be dimensioned with respect to the prospective fault current for a reliable and fast current commutation.

Fig. 5 shows the commutation time of $\Delta t_{AB\text{-}MB}$ versus the equivalent snubber capacitance C_{snequ}. Parameters for the tested CCCB are listed in Table 4, except that C_{snequ} is varied from 0μF to 0.6μF. Increasing the snubber capacitance C_{snequ} results in the increased commutation time of $\Delta t_{AB\text{-}MB}$. The commutation time $\Delta t_{AB\text{-}MB}$ is approximate to 6μs if the C_{snequ} is designed as 0.28μF.

Fig. 6 shows the commutation time of $\Delta t_{AB\text{-}MB}$ versus the stray inductance of the auxiliary branch (L_{sAB}). Increasing the stray inductance L_{sAB} results in the increased commutation time of $\Delta t_{AB\text{-}MB}$.

Fig. 7 shows the voltage across the LCS during the commutation time of $\Delta t_{AB\text{-}MB}$ versus equivalent snubber capacitance C_{snequ} of LCS. Increasing the equivalent snubber capacitance C_{snequ} results in decreased voltage across the LCS.

From Fig. 5 and Fig. 7, it is concluded that there is a trade-off between the voltage rating requirement of LCS during the commutation period and the commutation time of $\Delta t_{AB\text{-}MB}$ for the dimension of the snubbers.

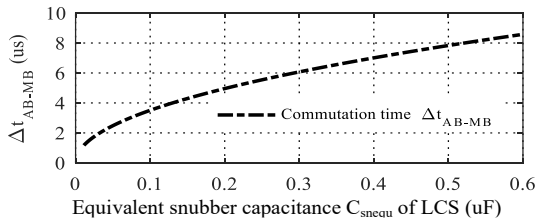


Fig. 5 Commutation time $\Delta t_{AB\text{-}MB}$ versus equivalent snubber capacitance C_{snequ}.

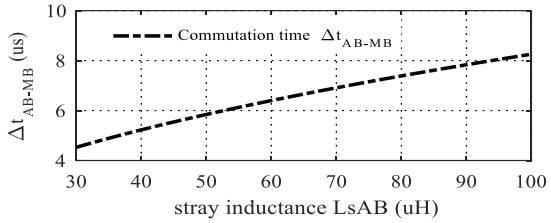


Fig. 6 Commutation time $\Delta t_{AB\text{-}MB}$ versus stray inductance of L_{sAB}.

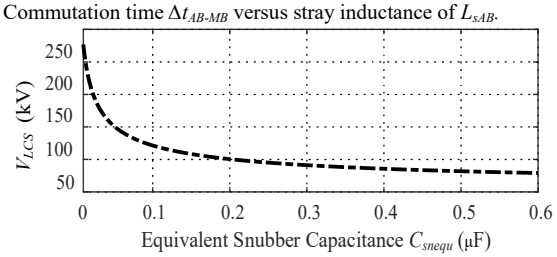


Fig. 7 The voltage across the LCS during the commutation time $\Delta t_{AB\text{-}MB}$ versus equivalent snubber capacitance C_{snequ}.

E. Impact of Stray Inductance on Voltage across LCS

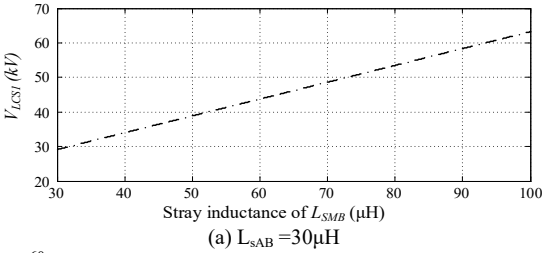
The stray inductances in the different branches have to be taken into account because they may cause commutation failure. The overvoltage induced by the stray inductances will also increase the voltage stress across the LCS(T_1) during the commutation period. According to references [25], the stray inductance is within the range of (30μH, 100μH).

V_{LCS1} is the voltage across the LCS during the time of $\Delta t_{AB\text{-}MB}$. Due to the large capacitance and high LCS voltage (>10kV), the V_c is assumed to be zero during the short commutation period. Therefore, V_{LCS1} can be obtained

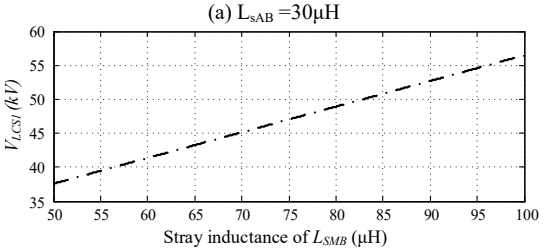
$$V_{LCS1} = L_{sMB}\frac{di_{main}}{dt} - L_{sAB}\frac{di_{mec}}{dt} = \frac{1}{C_{sn}}\int_0^{\Delta t_{AB\text{-}MB}} i_{mec}dt \quad (11)$$

Equation (11) shows that if the stray inductance (L_{sAB} or L_{sMB}) or the rise rate of current (di_{main}/dt or $|di_{mec}/dt|$) are increased, the voltage across the LCS (V_{LCS1}) will increase.

Fig. 8 shows the voltage V_{LCS1} versus the stray inductance L_{sMB} during the time of $\Delta t_{AB\text{-}MB}$. In Fig. 8(a), L_{SAB} is set as 30μH while L_{SMB} is varied from 30μH to 100μH. In Fig. 8(b), L_{SAB} is set as 50μH while L_{SMB} is varied from 50μH to 100μH. The other parameters of the tested CCCB are listed in Table 4. As indicated in Fig. 8, it can be seen that the larger the L_{sMB}, the higher the V_{LCS1}.



(a) L_{sAB} =30μH



(b) L_{sAB} =50μH

Fig. 8 The voltage across the LCS during the commutation time of $\Delta t_{AB\text{-}MB}$ versus stray inductance of L_{sMB}. (C_{sn}=5μF)

When the dc current i_{mec} decreases to zero, the order to open UFD is sent. As a conservative design, the UFD is modeled as an ideal switch with an operation time of ΔT [12]. Assuming that the V_c is totally undertaken by LCS during the time of ΔT. The V_{LCS2} is defined as the voltage across the LCS during the opening of UFD. Substituting ΔT into (6), the V_{LCS2} is calculated as

$$V_{LCS2} = Z_c I_{dctrip}\sin(\omega_0\Delta T) + V_{dcn}\left[1-\cos(\omega_0\Delta T)\right] \quad (12)$$

Fig. 9 shows the voltage V_{LsMB} across the stray inductance versus the L_{sMB} during the opening of UFD. Parameters for the tested CCCB are listed in Table 4, except that L_{sMB} is varied from 0μH to 300μH. As indicated in Fig. 9, the larger the L_{sMB}, the higher the V_{LsMB}. The V_{LsMB} is around 0.52kV during the opening of UFD when the L_{sMB} is as high as 300μH. However, the L_{sMB} of 300μH is considerably large, even though the voltage rating of capacitor is up to 480kV. The typical value of equivalent series inductance for a single capacitor with voltage rating of 2.8kV and capacitance rating of 9mF is in order of 10nH [26].

Fig. 10 shows that the L_{sMB} have a negligible influence on the voltage V_{LCS2} across the LCS during the opening of UFD.

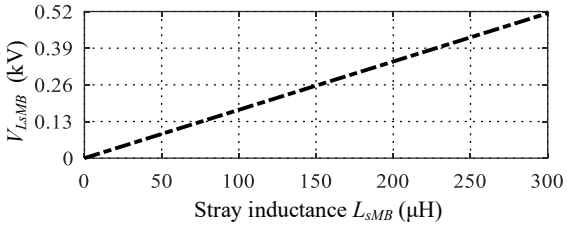


Fig. 9 The voltage across the stray inductance during the opening of UFD versus stray inductance of L_{sMB}.

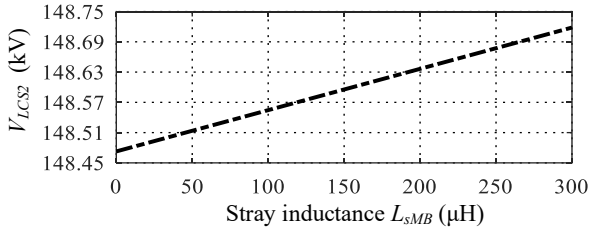


Fig. 10 The voltage across the LCS during the opening of UFD versus stray inductance of L_{sMB}.

To be concluded, the stray inductance per branch has a considerable influence on the voltage across LCS during the commutation process between the auxiliary branch and the main branch. However, they have a negligible impact on the voltage across LCS during the opening of UFD.

III. General Sizing Method of the CCCB

A. Dimensioning of the Capacitance

During the opening of UFD, the voltage V_c will be undertaken by UFD and LCS together. An arc may be induced in UFD if V_c increases too fast. Once the arc is induced, V_c is applied at LCS, which results in a significant voltage rating requirement of LCS. As a conservative design, LCS is dimensioned to undertake all V_c during the opening of UFD.

Fig. 11 shows the capacitance versus the internal current commutation time of the CCCB. Parameters for the tested CCCB are listed in Table 4, except that C is varied from 40μF to 100μF. Since less damping and a faster rate of rise of the dc fault currents, fast detection and clearance within a few milliseconds of dc fault current are required. In a HVDC grid, the DCCBs must begin to open and break the fault current in approximately 5ms [27]. Studies show that travelling wave protection can detect a dc fault within 2ms [28]. Therefore, the time for interrupting the fault, namely the internal current commutation time, is of 3ms. To achieve an internal current commutation time of 3ms, the commutation capacitance should be designed as 52μF for the CCCB with a dc voltage rating of 320kV. It should be pointed out that the internal current commutation time is not limited severely to 3ms. The shorter the fault detection time, the longer the acceptable internal current commutation time so long as the dc fault current can be interrupted within approximately 5ms. Consequently, the commutation capacitance of 60μF is also acceptable because of the relatively short internal current commutation time of approximately 3.21ms.

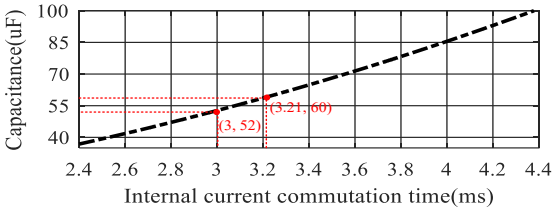


Fig. 11 Internal current commutation time versus commutated capacitance

B. Dimensioning of the Rating of LCS

The current rating of the LCS is equal to the dc load current in normal operation. Depending on the protection scheme, a certain time (relay time, typically on the order of tens of microseconds to a few milliseconds [8]) is required for the system-level relay to detect the fault, select the faulted line and send a trip order to the respective circuit breakers. LCS is exposed to the dc fault current during the relay time. Fig. 12 shows the relationship of V_{LCS} versus C. Parameters for the tested CCCB are listed in Table 4. A lower capacitance of C indicates a higher voltage rating of LCS, which leads to higher on-state power loss and cost. For the CCCB with a voltage rating of 320kV, the voltage rating of T_1 is 150kV if a capacitor of 60μF is selected.

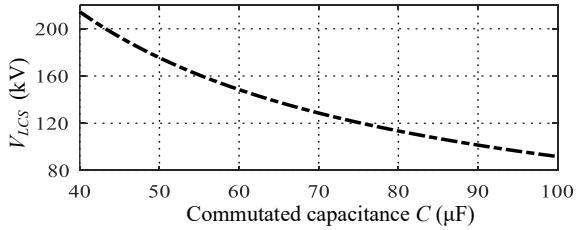


Fig. 12 Peak voltage of the LCS versus capacitance during the opening of *UFD*

Fig. 11 and Fig. 12 show that a higher C results in longer time to interrupt the dc fault current but a lower voltage rating of LCS and a lower C results in short time to interrupt the dc fault current but a higher voltage rating of LCS. There is a trade-off between the voltage rating of LCS and the interruption time for the dimension of the commutated capacitor.

C. Dimensioning of the Voltage Rating of the Diodes

To suppress the LC resonance caused by the C and the distributed parameters along the transmission lines during the fault clearance, a diode valve D is arranged in the main branch, as shown in Fig. 1.

After isolating the dc fault, V_c is maintained at the peak transient interruption voltage (TIV)[8]. The voltage across the diode valve is

$$V_D = (K_{\text{pro}} - 1)V_{\text{dcn}} \tag{13}$$

where $K_{pro}V_{dcn}$ is the protective level of the arresters. It is typically designed as 1.5 times the rated dc bus voltage. Voltage balance among the diodes is achieved by the sharing capacitors connected in parallel. A feasible candidate for the sharing capacitor is selected as 100pF [29]. As these sharing capacitors are significantly smaller than C, they are not considered in the design of CCCB.

For the bidirectional CCCB shown in Fig. 19, the voltage stress across the diode valve equals V_c.

D. Dimensioning of the Current Limiting Reactor

A larger L_{dc} is able to limit the fault current to smaller value and therefore reduce the charging effect of C. Fig. 13 shows the voltage stress across LCS versus different L_{dc} with C=60μF for a 320kV CCCB. The size of L_{dc} significantly impacts the required energy dissipation capability of the CCCB. The assessment of the energy dissipation capability is correlated with the peak fault current and system parameters, such as the L_{dc} and the maximum allowable fault neutralization time. Therefore, the value of the L_{dc} should be optimized by considering both the HVDC breaker requirements and the energy dissipation capability of the arresters.

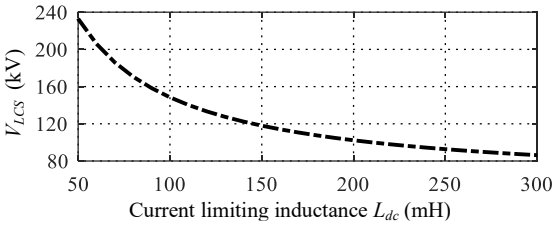


Fig. 13 Voltage stress across *LCS* versus L_{dc}

The total energy contributed by the L_{dc}, the transmission line inductances L_{line} and the voltage source in the HVDC system during the fault suppression period must be dissipated by the arrester banks in the DCCB[30]-[31]. Neglecting the fault resistance R_{flt}, by using the energy balance equation during dissipation period, the total energy dissipated by the arresters is calculated as

$$E_{arr} = (I_{\max}^2 \times L_{dc})/2 + \int_0^{t_c} v_{src}(t) \times i_{dc}(t) dt + (I_{\max}^2 \times L_{line})/2 \tag{14}$$

where I_{max} is the maximum current through CCCB. t_c represents the fault current suppression time (time interval between the peak fault current and the instant when the current has been lowered to leakage current [8]) and v_{src} is the voltage of the source in the HVDC system. The second term on the right side of (14) represents the energy supplied by the source. The magnitude of the source voltage during the interruption process significantly affects the amount of energy dissipation. The third

term on the right side of (14) represents the energy stored in the dc line inductances.

Assume that the DCCB is approximated as a constant voltage source with a voltage of V_{arr} (protective level of arrester) during the energy absorption. With this assumption, the *di*/*dt* is obtained as

$$di_{dc}/dt = (V_{dc} - V_{arr})/(L_{dc} + L_{line}) \quad (15)$$

The dc fault current during energy absorption can be expressed as

$$i_{dc} = \frac{(V_{dc} - V_{arr})}{(L_{dc} + L_{line})} t + I_{\max} \quad (16)$$

The fault current suppression time (t_c) can be determined by setting i_{dc}= 0

$$t_c = \frac{I_{\max}(L_{dc} + L_{line})}{(V_{arr} - V_{dc})} \quad (17)$$

Substituting (17) into (14), E_{arr} is obtained

$$E_{arr} = \frac{I_{\max}^2 \times (L_{dc} + L_{line}) \times V_{arr}}{2(V_{arr} - V_{dc})} \quad (18)$$

Fig. 14 shows the energy dissipated by the arrestor versus L_{dc} and I_{max}. Increasing the maximum current I_{max} or the inductance (L_{dc}+L_{line}) results in increased energy dissipation. To be noted, the varistor voltage V_{arr} has a minimum value to guarantee the interruption of fault current.

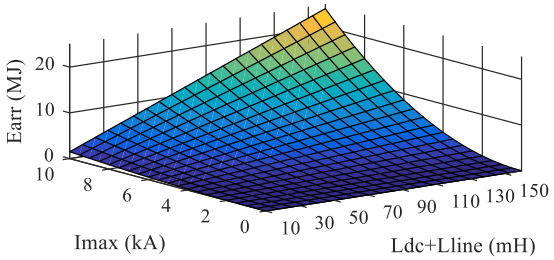


Fig. 14 Total energy dissipated by the arrestor versus (L_{dc} + L_{line}) and I_{max}

IV. Re-Closure of the CCCB

A. Reclosing to Un-Loaded Transmission Lines

Assuming that UFD, S_2, T_1, and S_3 are initially in open state and the dc transmission lines are initially in un-loaded condition, S_2 will firstly be closed once receiving the closing order. Then, UFD and T_1 will be closed successively. Since the transmission lines are un-loaded, there might be inrush current charging the distributed capacitance along the transmission lines. Because of the large current-limiting reactor L_{dc}, this inrush current will not cause overcurrent to T_1.

To ensure that the CCCB will not be closed to a permanent dc fault, UFD will be closed only when the dc fault is cleared. Fig. 15 shows the equivalent circuit when S_2 is closed and UFD is still opened. In steady state, the C is charged up to

$$V_C^{chg} = \frac{C_{line}}{C + C_{line}} V_{dcn} \quad (19)$$

where V_c^{chg} is the voltage across commutation capacitor. The typical transmission line capacitance is (1.39-1.23)μF/100km for overhead lines (OHLs) with a voltage rating of ±(200-400)kV[32]. Taking an average of 1.31μF/100km as an example, V_c^{chg} will reach as high as $0.1V_{dcn}$ when the length of the OHL is greater than 500km. The shorter the transmission line, the lower the V_C^{chg}. Therefore, the criterion to make sure that the fault has been cleared is that V_{line} is higher than a certain threshold value ($0.7V_{dcn}$ for example).

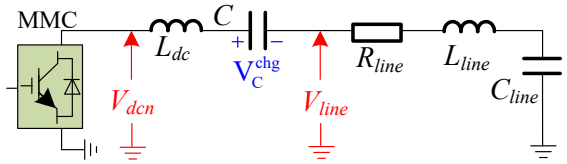


Fig. 15 Equivalent circuit when S_2 is closed and UFD is in open state

B. Reclosing to Pre-Charged Transmission Lines

Upon detecting that V_{line} of a CCCB is near the rated dc voltage, S_2 will firstly be closed. The *C* will be charged to (V_{dc}-V_{line}) if V_{dc} is higher than V_{line}.

Once the contacts of S_2 have been firmly connected, UFD will be closed. T_1 still remain in the open state. Since the off-state resistance of T_1 is high, even if (V_{dc}-V_{line})>0, the arc will not be induced in UFD. After closing UFD, T_1 is turned on, and dc current flows through T_1.

After closing S_2, *C* will be charged if V_{dc} is higher than V_{line}. During the Δ*T* of closing UFD, the maximum voltage across *C* is calculated according to (6), which is

$$\Delta V_c = (V_{dc} - V_{line})[1 - \cos(\omega_0 \Delta T)], (V_{dc} - V_{line}) > 0 \quad (20)$$

ΔV_c is approximately 3.0kV if (V_{dc}-V_{grid}) is 10kV. Equation (20) can be used as another equation to dimension the voltage rating of valve T_1.

C. CCCB with Fast-Closing Capability

To enable fast re-closing of the CCCB without waiting for discharge of the dc capacitor, a CCCB with dual capacitors is proposed as shown in Fig. 16. Fig. 16 is similar to Fig. 1 except that the main branch implements two capacitors C_a and C_b. Each capacitor is connected in series with the mechanical switches S_{4a} and S_{4b}, respectively.

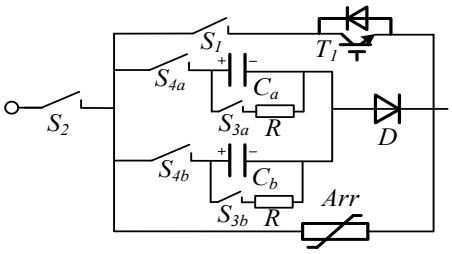


Fig. 16 Unidirectional CCCB with fast-closing capability

In normal operation, S_{4a} is closed, and S_{4b} is opened. On the first trial of opening of the CCCB, T_1 and *UFD* will be opened, and C_a will be charged up to $K_{pro}V_{dcn}$ during isolation of the dc fault. After the dc current drops to zero, S_{4a} will be opened to isolate C_a. To reclose the CCCB, S_{4b} will firstly be closed, and then S_1 and T_1 will be closed.

V. Extended Topology of CCCB

To further reduce the semiconductor cost and on-state power loss of the auxiliary branch in the CCCB, several extended topologies are proposed as shown in Fig. 17 and Fig. 19.

Fig. 17 is similar to Fig. 1, except that a thyristor valve T_2 is connected in series with T_1. Compared with Fig. 1, the LCS is composed of IGBT valve T_1 and thyristor valve T_2. The advantages of the arrangement of T_1 in series with T_2 are as follows: 1) the cost of the power electronic devices in the LCS is reduced; and 2) the on-state power loss of the auxiliary branch in the CCCB is reduced. When the LCS receives the opening order, T_1 will firstly be turned off because of its fast turn-off speed. Subsequently, the current flowing through the auxiliary branch drops to zero after a commutation time, which ensures that T_2 can be turned off. For a thyristor, the typical turn-off time is in the range of 40μs-800μs [33][34]. As a result, the capacitor voltage is fully applied to T_1 during the turning off of T_2. After turning off T_2, the capacitor voltage is undertaken by both T_1 and T_2.

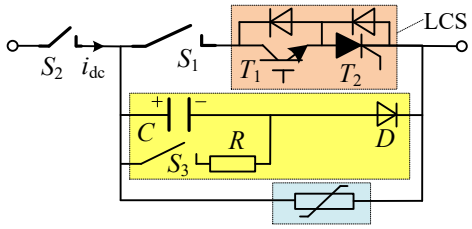


Fig. 17 Alternative unidirectional CCCB

Fig. 18 shows the voltage stress of T_1 (V_{T1_IGBT}) during turning off of T_2. A longer turn-off time (T_{off}) of T_2 or a smaller capacitance of C indicates a higher V_{T1_IGBT}. Since the V_{T1_IGBT} is relatively small during turn off of T_2, a small quantity of IGBT can be adopted at T_1. The voltage rating of T_2 can be dimensioned according to (6).

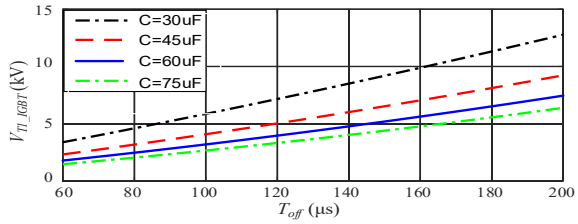


Fig. 18 Peak voltage stress of T_1 during turn off of T_2

Series connection of T_1 and T_2 significantly reduces the cost of the LCS since the thyristors usually have a higher voltage rating and lower cost than IGBTs. Additionally, the on-state power loss of the LCS can be decreased.

Fig. 19 shows the topology of bi-directional CCCB. Single-phase uncontrolled rectifier bridges are implemented at the main branch and auxiliary branch. They are connected in parallel with the commutation capacitors and LCS, respectively. The diode bridge configuration allows CCCB to interrupt the bidirectional dc fault current without doubling the cost of the power electronics devices.

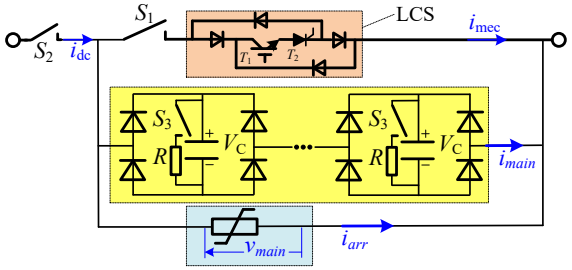


Fig. 19 Bidirectional topology of the CCCB

VI. Power Loss and Cost Assessment of the CCCB

The bidirectional CCCB shown in Fig. 19 is used to evaluate the power loss and cost in this section. The main parameters of the CCCB are disclosed in Table 4.

A. Power Loss Assessment of CCCB

Fig. 8 and Fig. 18 shows that the peak voltage across T_1 is approximately 36kV during the dc fault clearance phase when C is selected as 60μF. To reduce the conduction power loss and improve the reliability, a matrix of 3x3 IGBT positions [9] is chosen for the T_1. Reference [11] depicts the withstand voltage of one matrix is as high as 9kV. 4 matrices are sufficient for T_1 to achieve the requirements of the voltage rating of approximately 36kV. The IGBT chosen for T_1 is the 5SNA2000K450300, which is rated at 4.5kV/2kA. The conduction loss of a matrix is equal to 22.6kW[11].

Fig. 12 shows that the peak voltage across the LCS is on the order of 150kV during the opening of UFD if C is selected as 60μF. T_1 and T_2 will share this peak voltage of 150kV. Since the thyristors typically have a lower on-state voltage drop and cost than the IGBTs, the number of IGBTs should be as few as possible to reduce the cost and on-state power loss at the normal operation. Therefore, as a conservative design, the peak voltage stress across the T_2 is dimensioned to be 114kV. The voltage distribution between T_1 and T_2 can be achieved by the rational design of the RCD snubber and voltage-sharing circuits connected in parallel with T_1 and T_2. To achieve the requirement of the voltage rating of 114KV, considering a certain voltage safety margin, 26 matrices of 3x3 SCR positions with a maximum withstand voltage level of 4.5kV per matrix are sufficient for T_2. The thyristor (SCR) chosen for T_2 is 5STF23H2040 rated at 2kV/2.322kA because of its optimized turn-off time of 60μF, the favorable forward characteristics (V_{TSCR}=1.516V, r_{TSCR} = 0.111mΩ).

The SCR matrix requirement specifications, including the safety margins of 33%, are provided in Table 1. The conduction loss of SCR of T_2 is calculated as

$$P_{T2} = N_{SCR\_matrix} \times 3 \times i_{dc} \times (V_{TSCR} + r_{TSCR} \times i_{dc}/3) \qquad (21)$$

where N_{SCR_matrix} is the number of matrices connected in series. According to (21), the component loss of T_2 is approximately 110.2kW.

Table 1 Requirement specifications for the SCR matrices for T_2

Requirements	*Value*
Nominal current /kA	2.0
Maximum continuous current/kA	2.6
Maximum current level during commutation/ kA	8
Maximum transient voltage stress during commutation/ kV	114
the number of matrix connected in series/ N_{matrix_T2}	26

Table 2 Requirement specifications for the diode valve

Requirements	*Value*
Nominal current/kA	2
Maximum continuous current/kA	2.6
Maximum current level during commutation/kA	8
Maximum transient voltage stress during commutation/ms	150
Number of matrixes connected in series for one diode valve/N_{matrix_dio}	15

A single-phase uncontrolled rectifier is arranged in parallel with the LCS as shown in Fig. 19. The diode chosen for the diodes valves is 5SDD20F5000, which is rated at 5kV/1.978kA. To accomplish the requirement of a voltage of 150kV, 15

matrices of 3x3 diode positions connected in series are placed in one diode valve. The total conduction loss of the single-phase uncontrolled rectifier is expressed as

$$P_{REC} = N_{D\_matrix} \times i_{dc} \times (6\,V_{Tdio} + 2r_{Tdio} \times i_{dc}) \quad (22)$$

where N_{D_maxtri} is the number of matrices and V_{Tdio} and r_{Tdio} are the threshold voltage and forward slope resistance of a single diode, respectively. According to (22), the power loss of the diode valve is 91.5kW.

In conclusion, the percent total power loss for the CCCB can be expressed as

$$\eta = \frac{P_{REC} + P_{T2} + P_{T1}}{320kV \times 2kA} = 0.047\% \quad (23)$$

B. Cost Comparison of Different Hybrid DCCBs

Three types of DCCBs, the hybrid DCCB proposed by ABB[9], the hybrid DCCB implementing the H-bridge topology described in [13], and the bidirectional CCCB shown in Fig. 19, are used for a rough cost comparison. It is assumed that all the three DCCBs use the same fast dis-connector and surge arrester and the cost of fast dis-connector and surge arrester are not considered in the comparison. The price of IGBTs, capacitors and thyristors are assumed as follows:

i. The price of a single IGBT, 5SNA2000K450300, is K_{IGBT}.
ii. The price of a single thyristor, 5STF23H2040, is K_{SCR}=0.1K_{IGBT}.
iii. The price of a single diode, 5SDD20F5000, is K_{DIO}= 0.26K_{IGBT}.
iv. The price of a single capacitor for hybrid DCCB implementing the H-bridge topology, 3kV/7μF is approximately K_{CAP1}= 0.3K_{IGBT}.
v. The price of a single capacitor for CCCB, 2.8kV/12mF is approximately K_{CAP2}= 0.7K_{IGBT}.

The voltage safety factor of power electronics devices is selected as 33%. The rated voltage and rated current of the three types of DCCBs are 320kV and 2.7kA, respectively.

The semiconductor cost of the LCS and main branch of the hybrid DCCB proposed by ABB[9] is

$$K_{ABB} = 696K_{IGBT} \quad (24)$$

The semiconductor cost of the LCS and main branch for the hybrid DCCB implementing the H-bridge topology[13] is

$$K_{HBridge\_CB} = 690K_{IGBT} + 172K_{CAP} = 742K_{IGBT} \quad (25)$$

The semiconductor cost of the LCS and the cost of capacitors of the main branch of the CCCB is

$$K_{CCCB} = 36K_{IGBT} + 104K_{SCR} + 1020K_{DIO} + 200K_{CAP2} = 452K_{IGBT} \quad (26)$$

Table 3 summarizes the comparison of the three types of DCCBs. Although CCCB has higher operational power loss, it's cost is lower than the other two DCCBs. Power loss of CCCB is also significantly lower than the solid state DCCB, which has a typical power loss ratio of 0.2%[1].

Since a large capacitor is used in the main branch, the volume of CCCB will be larger than that of hybrid DCCB proposed by ABB [9], but smaller than that of hybrid DCCB proposed by ALSTOM[10].

Table 3 Comparison of the three types of DCCBs

	Hybrid DCCB (ABB)	Hybrid DCCB (SGRI)	CCCB
Rated voltage	320kV	320kV	320kV
Rated current	2.7kA	2.7kA	2.7kA
Interruption capability	16kA	15kA	16kA
Internal current commutation time	2.4ms	3ms	3.21ms
Power loss (%)	< 0.01%	< 0.01%	0.039%
Investment cost of the LCS and main branch (transfer branch)	100%	107%	64.9%

VII. Simulation Verifications

A. Simulations with CCCB interfaced to stiff DC battery

To verify the performance of the CCCB, the test system shown in Fig. 20 is firstly simulated. In Fig. 20, the CCCB is connected to a stiff 320kV battery. The nominal dc current is 1.6kA. The switch S_{flt} is closed to initiate the fault. Such stiff DC batter imposes most stringent requirements on DCCB [8][30].

Table 4 lists parameters of the tested CCCB. The topology shown in Fig. 1 is simulated. The switch S_{flt} is closed at 0.1s to simulate a permanent low-resistance fault. Once the dc current exceeds 2kA, trip order of the CCCB is sent. The T_l in LCS consists of 18 matrices of 3x3 IGBT positions with parallel RCD snubbers and a static voltage-sharing circuit. The RCD snubber used for each IGBT was set to 8Ω/5μF[23][24], that is, the equivalent snubber capacitance of C_{snequ} of LCS is designed as 0.277μF. And the resistance of the static voltage-sharing circuit for each IGBT is 450kΩ. The stray inductances per branch were assumed to be 50μH. The simulation results are shown in Fig. 21.

Table 4 Parameters of the tested CCCB

Parameters	*Value*
Rate dc voltage V_{dcn}/kV	320
Rated dc current I_{dcn}/kA	1.6
Limiting inductance L_{dc}/mH	100
Capacitance C/μF	60
Operating time of the UFD S_1 T_{mec}/ms	2
Switch off time of the residual disconnector S_2 T_{res}/ms	40
Rated voltage of the diode valve V_{Dn}/kV	480
Rated voltage of the IGBT valve V_{IGBTn}/kV	150
Rated voltage of the capacitor V_{Cn}/kV	480
Rated voltage of the arrester V_{arr}/kV	243
Maximum breaking current of *UFD* without arc I_{mec}/kA	0.01[12]
RCD Snubber Capacitance for IGBT C_{sn}/μF	5
RCD Snubber resistance for IGBT R_{sn}/Ω	8
Static voltage-sharing resistance for IGBT R_s/kΩ	450
The stray inductance of the auxiliary branch L_{sAB}/μH	50
The stray inductance of the main branch L_{sMB}/μH	50
The stray inductance of the absorb branch L_{sB}/μH	50

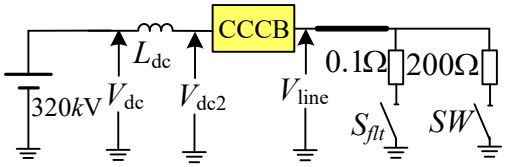


Fig. 20 Tested single-terminal system

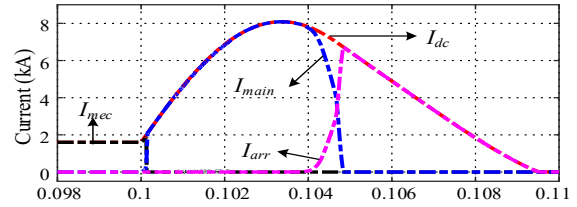
Fig. 21 (a) shows the currents i_{dc}, i_{mec}, i_{main} and i_{arr}. Upon receiving the trip order, i_{mec} decreases to zero after a commutation time of $\Delta t_{AB\text{-}MB}$. Then, i_{dc} transfers to the main branch to charge C. The current in the main branch i_{main}

increases rapidly. In the meantime, the voltage V_c across the commutated capacitor increases with a slow slope, as shown in Fig. 21 (b). Once V_c reaches the protective level (typically $1.5V_{dcn}$) of the arrester banks, the arresters conduct to absorb the residual energy. The dc current i_{dc} starts to decrease when the V_c reaches to V_{dc}. When i_{dc} is less than the residual current of the dis-connector S_2 (typically 0.001kA), S_2 will open and provide a reliable insulation gap between the stiff 320kV battery and CCCB to protect the arrester banks from thermal overload caused by the leakage current. From Fig. 21 (a), it can be seen that the peak value of i_{dc} is approximately 8kA, which is in line with the calculated value shown in Fig. 3.

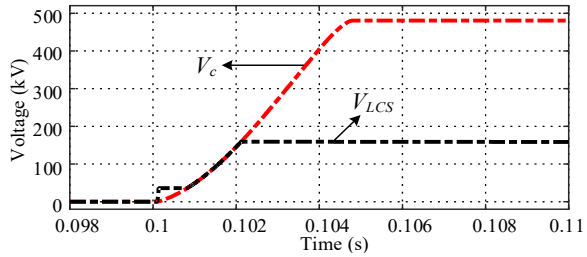
Fig. 21 (b) shows the voltage in the CCCB during the fault clearance. The peak value of 480kV of V_c is equal to the protective level of the arrester banks. And V_c is maintained at 480kV until the discharging branch is closed. The V_{LCS} is approximately 37kV during the commutation between the auxiliary branch and the main branch because of the stray inductance and the high $|di_{mec}/dt|$. The V_{LCS} is approximately 150kV during the opening of UFD, which is in line with the calculated value shown in Fig. 13.

Fig. 21 (c) shows the current of CCCB during the commutation time of $\Delta t_{AB\text{-}MB}$. The i_{dc} is almost constant during the short commutation period, indicating the assumption in section II.B is valid. The $\Delta t_{AB\text{-}MB}$ is approximately 8μs when the RCD snubber used for each IGBT was set to 8Ω/5μF. As shown in Fig. 6, the $\Delta t_{AB\text{-}MB}$ is approximately 6μs when the RCD snubber was set to 5μF. However, this minor difference is acceptable.

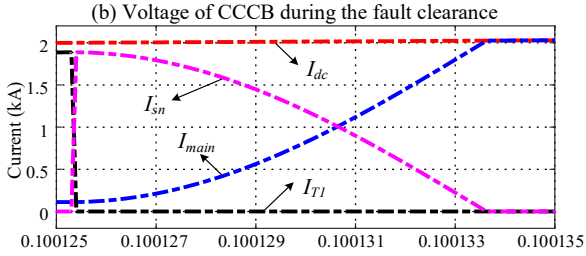
Fig. 21 (d) shows the voltage of capacitor in the main branch during the commutation between the auxiliary branch and the main branch. The V_c is approximate to zero during the commutation time of $\Delta t_{AB\text{-}MB}$, indicating the assumption in section II.E is valid.



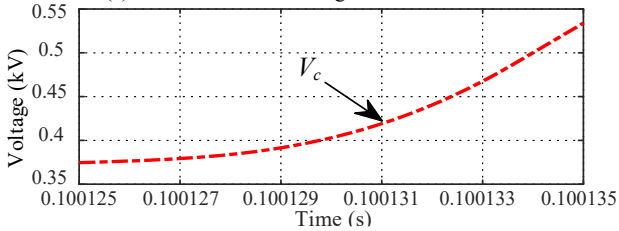
(a) Current in the CCCB during the fault clearance



(b) Voltage of CCCB during the fault clearance



(c) Current of CCCB during the time of $\Delta t_{AB\text{-}MB}$.



(d) The voltage of capacitor in the main branch during the time of $\Delta t_{AB\text{-}MB}$.

Fig. 21 Simulation of the breaking capacity of the CCCB

To further test the calculation in section II, the value of the commutated capacitance is varied from 40μF to 100μF. Fig. 22 shows the peak fault currents versus different capacitances under simulation and analytical calculation. From Fig. 21, it can be seen that the simulation results match the calculation results well.

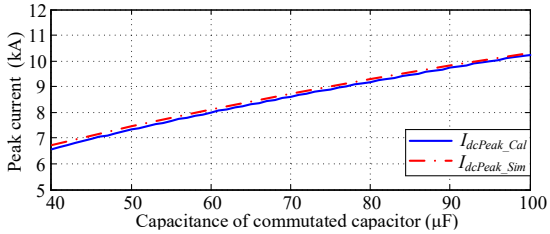


Fig. 22 Comparisons of peak fault currents between the simulation results and the calculation results

B. Application of the CCCB in a MTDC

The bidirectional CCCB shown in Fig. 19 is further tested in a four-terminal HVDC grid, as shown in Fig. 23. The dc voltage rating of the MMC is set as ±320kV. Each of the MMC employs half-bridge sub-modules. The 100-km overhead lines are modeled with frequency-dependent phase model provided by PSCAD/EMTDC.

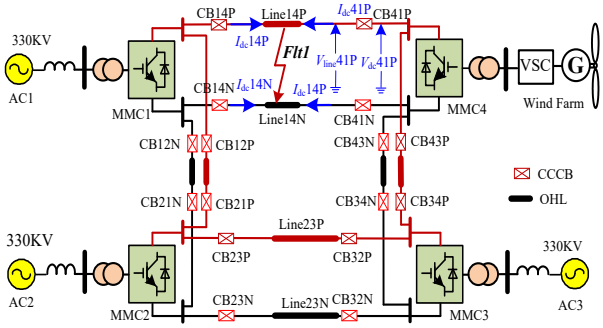


Fig. 23 Tested 4-terminal MTDC with the CCCB

MMC1 operates as an inverter in dc voltage control mode. MMC4 operates as a rectifier in ac voltage control mode. The 3-level cascaded controller proposed in [35] is applied to MMC2 and MMC3. The 3-level cascaded controller enables both MMC2 and MMC3 to contribute to the control of the local dc voltage in the dc grid in case the local active power controller fails. The current-limiting reactor installed at each CCCB is 100mH [9].

1) *Traveling Wave dc fault Detection*

As shown in Fig. 24, a fault detection method based on rate of change of voltage (ROCOV) as described in [31] is employed in this paper to discriminate an internal dc fault and external dc fault. The time constant of T_d is 200μs, and the

threshold of $|dV_{dc}/dt|$ is 1000kV/ms. MMCs will be blocked if the arm current is higher than 2 times the rated value.

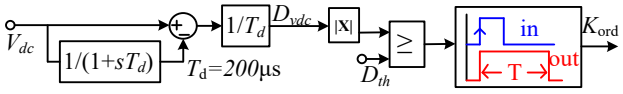


Fig. 24 Fault-detection logic of the CCCB

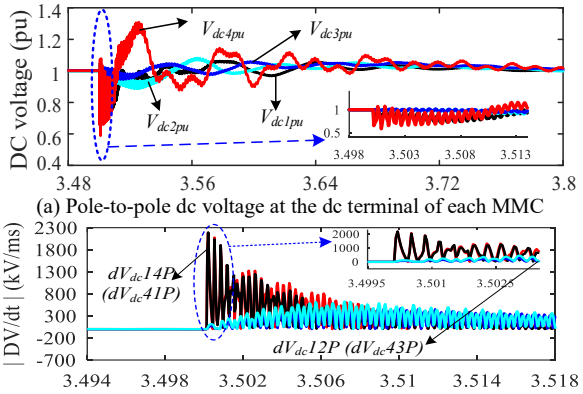
2) *Verification of the Breaking Capability of the CCCB*

To verify the breaking capability of the CCCB in a four-terminal HVDC grid as shown in Fig. 23, a pole-to-pole dc fault is applied at *Flt1* at 3.5s. The fault location is approximately 50km away the dc terminal of MMC1.

Fig. 25(a) shows the dc bus voltages of MMC1-MMC4. The dc voltages V_{dc1} and V_{dc4} rapidly decrease to 0.7pu when the fault voltage travelling wave propagates to the dc bus. The decrease of V_{dc2} and V_{dc3} is relatively small because the traveling wave is damped by the L_{dc} and the distributed parameters along the transmission lines.

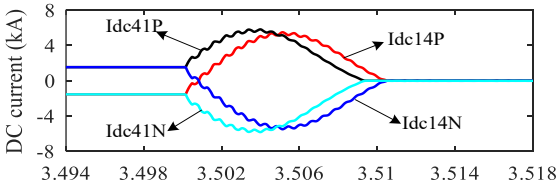
Fig. 25(b) shows the voltage differential dV_{dc} of the positive pole to the ground voltage at the line side of the CCCBs. dV_{dc} is close to zero in the steady state. The maximum values of $|dV_{dc}14P|$ (or $|dV_{dc}41P|$) and $|dV_{dc}12P|$ (or $|dV_{dc}43P|$) are 2150kV/ms and 500kV/ms during 3.5-3.51s. Therefore, Line14P and Line14N will be tripped selectively.

Fig. 25(c) shows the line currents of CB41P, CB41N, CB14P and CB14N during the operation of the CCCB. When a fault occurs, the dc current rapidly rises because of the low equivalent impedance in the dc grid. The maximum values of $I_{dc}14P$ and $I_{dc}41P$ are 5.2kA and 5.7kA, respectively. At 3.504s, $I_{dc}41P$ reaches the maximum value of 5.2kA.



(a) Pole-to-pole dc voltage at the dc terminal of each MMC

(b) Differential of the positive pole-to-ground voltage at the line side of the CCCB



(c) DC current in a faulty transmission line

Fig. 25 DC grid response to a pole-to-pole dc fault

3) *Response to Reclosing the Transmission Lines*

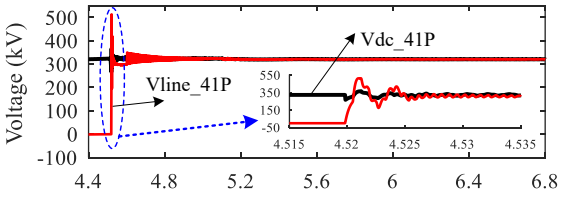
To investigate the reclosing of the transmission lines, the dc fault is cleared at 4s. CB41P and CB41N are arranged to reclose at 4.5s. Since the voltage of the dc line capacitors is discharged to zero, CB41P and CB41N are regarded as having reclosed to un-loaded transmission lines. At 5s, CB14P and CB14N are arranged to reclose. Since the voltage of the dc line has been charged-up, CB14P and CB14N can be regarded as having reclosed to pre-charged transmission lines.

The measuring positions of V_{dc}_41P and V_{line}_41P are also shown in Fig. 23. As CB41P and CB41N are reclosed to the un-loaded transmission line, the MMC4 will charge capacitor C and the distributed capacitor C_{line} of line14P and line14N.

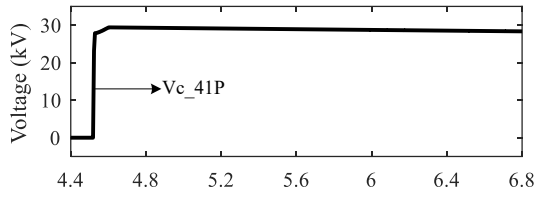
Fig. 26 (a) shows the dc voltage in CB41P. A damped oscillation of V_{line}_41P is observed during 4.52-5.0s, which results from the current-limiting reactor and the stray inductors and capacitors along the transmission lines. The overshoot of V_{line}_41P is up to 56% of the rated dc voltage. The overvoltage with a peak value of 500kV results in a challenge to the insulation coordination. To suppress the overvoltage in the reclosing procedure, an arrester with a rating voltage of 320kV is placed at the line side of each CCCB.

Fig. 26 (b) shows the capacitor voltage in CB41P. Once CB41P and CB41N are closed to un-loaded lines, the voltage (V_C_41P) across the commutated capacitor C will be charged up to 28kV at 4.526s. Furthermore, a surge current with a peak value of up to 0.9kA is observed in I_{dc}_41P at 4.5205s.

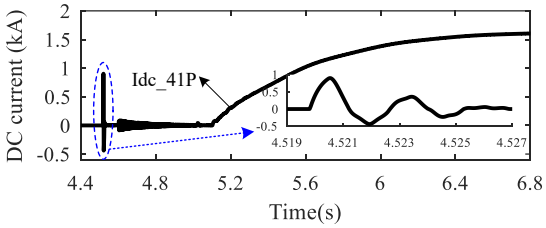
Fig. 26 (c) shows the dc current in CB41P. To recover the dc power flow in the pre-charged line14P and line 14N, CB14P and CB14N are reclosed at 5s. At 5.1s, I_{dc}_41P starts to increase gradually. Eventually, the nominal rating of 1.6kA is achieved at 6.8s. When damped by the current-limiting reactor, it takes 1.7s to recover the steady-state value of the I_{dc}_41P.



(a) DC voltages in CB41P



(b) Capacitor voltage in CB41P



(c) DC current in CB41P

Fig. 26 Reclosing to transmission lines

4) *Reclose to Transmission Lines with a Low-Resistance Fault*

To investigate the response of reclosing to transmission lines with a low-resistance fault, CB41P and CB41N are reclosed at 4.5s. The fault resistor R_{flt} is 0.1Ω. As the dc fault remains, CB14P and CB14N will receive a signal from the protection system to prohibit reclosing. Upon receiving the reclosing signal, the residual dis-connectors S_2 of CB41P and CB41N are

closed after waiting for 20ms to ensure that the contacts are firmly connected. The dc voltage (V_{dc4}) of MMC4 is applied to the distributed line capacitor C_{line}, commutated capacitor C and fault resistor R_{flt} because the dc fault remains.

Fig. 27 (a) shows the dc voltages in CB41P. When S_2 is closed, C_{line} and L_{dc} will undertake V_{dc_41P} together. The pole-to-ground voltage V_{line_41P} and the voltages across the L_{dc} (V_{Ldc}) reach 140kV and 250kV, respectively. Subsequently, V_{line_41P} and V_{Ldc} gradually decrease to zero.

Fig. 27 (b) shows the capacitor voltage (V_{C_41P}) in CB41P. After 4.52s, V_{C_41P} increases to an overvoltage of up to 460kV within 10ms.

As shown in Fig. 27 (c), a transient inrush current with a peak value of 5.2kA is observed in I_{dc_41P} at 4.525s, which results from the charging of capacitor C. I_{dc_41P} increases to its maximum at the instant V_{C_41P} equals V_{dc_41P}. Subsequently, I_{dc_41P} decreases to zero, and V_{C_41P} increases to its maximum value of 460kV. Once I_{dc_41P} is near zero, S_2 will open to protect the arresters from thermal overload.

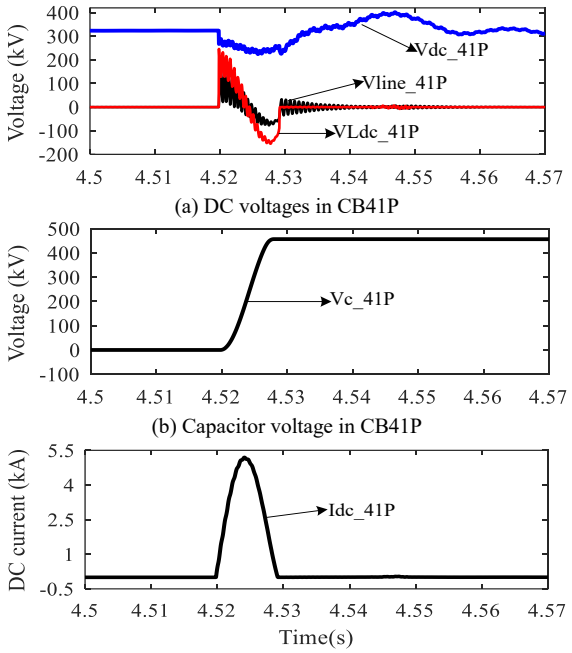


Fig. 27 Reclosing to the transmission line with a low-resistance fault

VIII. Conclusion

This paper proposes a capacitor commutated dc circuit breaker (CCCB) to significantly reduce the investment cost of hybrid DCCBs and facilitate their popularization in engineering applications. Three extended topologies of CCCB are proposed. Taking the CCCB with a voltage rating of 320kV, rated current of 2kA and interruption capability of 16kA as an example, the analysis and calculation results show that the power loss of the bidirectional CCCB is 0.047%. The total of semiconductor cost and capacitor cost of CCCB is about 64.9% of ABB's hybrid DCCB. Extensive simulations verified technical feasibility of the CCCB. Analysis indicate that the stray inductance on each branch has a considerable influence on the dimensioning of the CCCB and the interruption of fault current as well. There is a trade-off between a fast and reliable interruption and low capital cost.

The analysis of CCCB presented in this paper could be applied to the circuit breaker in [14] and so on. Further work will take into account the optimal design of the snubbers for the LCS and the optimal dimension of other types of CCCB.

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